

REMARKS

Applicants appreciate the Examiner's allowance of Claims 17-19. Except as discussed below, Applicants have made minor amendments to the claims to correct informalities therein. These amendments are not in response to a patentability rejection.

Applicants have the following response to the Examiner's only rejection in the Office Action.

Claim Rejections - 35 USC §102

In the Office Action, the Examiner rejects Claims 1, 5, 9, 13, 20 and 21 under 35 USC §102(b) as being anticipated by Hashimoto (US 5,825,204). This rejection is respectfully traversed.

While Applicants traverse this rejection, in order to advance the prosecution of this application, Applicants have amended independent Claims 1, 5, 9, 13, 20 and 21 as follows:

Claims 1 and 5 have been amended to recite "wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND, and wherein the second input terminals of the first and second NANDs are directly connected to first and second signal lines, respectively."

Claim 9 has been amended to recite "a source driver which inputs a clock signal, a start pulse and a video signal and outputs a plurality of signals to a plurality of source signal lines in accordance with the clock signal, the start pulse and the video signal" and "wherein the plurality of signals outputted to the plurality of source signal lines are inputted to a plurality of input terminals" (of an inspecting circuit).

Claim 13 has been amended to recite "a gate driver which inputs a clock signal and a start pulse and sequentially outputs a select pulse to a plurality of gate signal lines in accordance with the

clock signal and the start pulse” and “an inspecting circuit including a plurality of latch circuits sampling a signal for inspection in accordance with the select pulse,” and “a plurality of input terminals to which output signals from the plurality of latch circuits are inputted.”

Claim 20 has been amended to recite “simultaneously inputting a signal to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i -th NAND is inputted to a second input terminal of $(i+1)$ th NAND.”

Claim 21 has been amended to recite “simultaneously inputting each of sampled signals to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i -th NAND is inputted to a second input terminal of $(i+1)$ th NAND.”

Hashimoto does not disclose or suggest the above recited features of independent Claims 1, 5, 9, 13, 20 and 21. Accordingly, these independent claims and the claims dependent thereon are patentable over Hashimoto, and it is respectfully requested that this rejection be withdrawn.

Conclusion

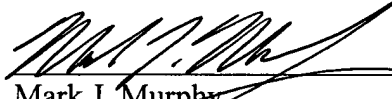
It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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